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PATENT
Dkt. STL11280

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Wayne L. Felts**
Assignee: **SEAGATE TECHNOLOGY LLC**
Application No.: **10/606,090** Group No.: **2116**
Filed: **June 26, 2003** Examiner: **James Trujillo**
For: **TRANSITIONING FROM STARTUP CODE TO APPLICATION CODE DURING INITIALIZATION OF A PROCESSOR BASED DRIVE**

Mail Stop Appeal Briefs – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION--37 C.F.R. § 41.37)

1. Transmitted herewith, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on January 12, 2007.

2. STATUS OF APPLICANT

This application is on behalf of other than a small entity.

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. § 41.20(b)(2), the fee for filing the Appeal Brief is:

other than a small entity	$500.00
Appeal Brief fee due	**$500.00**

4. EXTENSION OF TERM

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

Applicant petitions for an extension of time under 37 C.F.R. § 1.136 (fees: 37 C.F.R. § 1.17(a)(1)-(5)) for four months:

Fee: $1,590.00

If an additional extension of time is required, please consider this a petition therefor.

5. TOTAL FEE DUE

The total fee due is:

Appeal brief fee	$500.00
Extension fee (if any)	$1,590.00
TOTAL FEE DUE	**$2,090.00**

6. FEE PAYMENT

Authorization is hereby made to charge the amount of $2,090.00 to Credit card as shown on the attached electronic credit card information authorization.

7. FEE DEFICIENCY

If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 06-0540.

Date: 7/12/07

Respectfully submitted,

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Application No.:	**10/606,090**	Group Art Unit:	**2116**
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ATTENTION: Board of Patent Appeals and Interferences

Sir:

APPELLANT'S BRIEF

This Brief is in furtherance of the Notice of Appeal that was filed in this case on January 12, 2007. The required fees, petition for extension of time for filing this Brief, and the authority and time limits established by the Notice of Appeal are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains these items under the following headings, and in the order set forth below:

I. REAL PARTY IN INTEREST
II. RELATED APPEALS AND INTERFERENCES
III. STATUS OF CLAIMS
IV. STATUS OF AMENDMENTS
V. SUMMARY OF CLAIMED SUBJECT MATTER
VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL
VII. ARGUMENT
VIII. CLAIMS APPENDIX
IX. EVIDENCE APPENDIX
X. RELATED PROCEEDINGS APPENDIX

I. REAL PARTY IN INTEREST

The real party in interest in this Appeal is Seagate Technology LLC.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this Appeal.

III. STATUS OF CLAIMS

The status of the claims in this application is:

Claim	Status
1. (Original)	Independent.
2. (Original)	Depends from claim 1.
3. (Original)	Depends from claim 1.
4. (Original)	Depends from claim 3.
5. (Original)	Depends from claim 4.
6. (Original)	Depends from claim 1.
7. (Original)	Depends from claim 6.
8. (Previously presented)	Independent.
9. (Original)	Depends from claim 8.
10. (Original)	Depends from claim 8.
11. (Original)	Depends from claim 10.
12. (Original)	Depends from claim 8.
13. (Original)	Depends from claim 12.
14. (Previously presented)	Independent.
15. (Original)	Depends from claim 14.
16. (Original)	Depends from claim 14.
17. (Original)	Depends from claim 14.
18. (Original)	Depends from claim 17.
19. (Previously presented)	Depends from claim 1.
20. (Previously presented)	Depends from claim 1.

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application: 1-20.

B. STATUS OF ALL THE CLAIMS

1. Claims canceled: None.
2. Claims withdrawn from consideration but not canceled: None.
3. Claims pending: 1-20.
4. Claims allowed: None.
5. Claims rejected: 1-20.
6. Claims objected to: None.

C. CLAIMS ON APPEAL

Claims now on appeal: 1-20.

IV. STATUS OF AMENDMENTS

No post-final amendments have been submitted.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The embodiments of the present invention as recited by the language of independent claims 1, 8 and 14 are generally directed to an apparatus and method for processor control of an electrical load.

Independent claim 1 generally features a method comprising controlling an electrical load (such as 106, 116 in FIG. 1) with a first code (such as in "BOOT ROM" 136, FIG. 3 and "MEM 1" 220 in FIG. 8) executed by a processor (such as 132 in FIG. 3) – see steps 1-2 in FIG. 8; step 254 in FIG. 9; and in the specification at page 11, lines 1-8 and page 15, lines 4-7. The method of claim 1 further generally comprises releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code (such as in "RAM" 134, FIG. 3 and "MEM 2" 222 during step 2 of FIG. 8) – see step 3 in FIG. 8; step 258 in FIG. 9; and in the specification at page 10, lines 16-23; page 11,

lines 20-25; and page 15, lines 9-11. The method of claim 1 further generally comprises reinstating processor control of the electrical load using the second code – see step 4 in FIG. 8; step 260 in FIG. 9; and in the specification at page 11, lines 26-31; page 13, lines 24-28; page 15, lines 11-14; page 16, lines 16-21.

Independent claim 8 generally features a method comprising using a processor (such as 132 in FIG. 3) to execute startup code (such as in "BOOT ROM" 136, FIG. 3) loaded into a memory location (such as "MEM 1" 220 in FIG. 8) to initiate operational control of an electrical load (such as 106, 116 in FIG. 1) – see steps 1-2 in FIG. 8; step 254 in FIG. 9; and in the specification at page 11, lines 1-8 and page 15, lines 4-7. The method of claim 8 further generally comprises continuing to operate the electrical load while processor operational control of the electrical load is temporarily suspended to load application code (such as from "MEM 2" 222, FIG. 8) to the memory location ("MEM 1" 220, FIG. 8) – see step 3 in FIG. 8; step 258 in FIG. 9; and in the specification at page 10, lines 16-23; page 11, lines 20-25; page 15, lines 9-11; and page 16, lines 22-25. The method of claim 8 further generally comprises resuming operational control of the electrical load using the application code - see step 4 in FIG. 8; step 260 in FIG. 9; and in the specification at page 11, lines 26-31; page 13, lines 24-28; and page 15, lines 11-14.

Independent claim 14 generally features an apparatus comprising an electrical load (such as 106, 116 in FIG. 1); a memory location (such as "MEM 1" 220 in FIG. 8); and a programmable processor (such as 132, FIG. 3) coupled to the memory location and adapted to control the electrical load, wherein during an initialization process (such as 250, FIG. 9) the processor executes startup code loaded into the memory location to initiate operational control of the load (such as steps 1-2 in FIG. 8 and step 254, FIG. 9) – see specification at

page 11, lines 1-8 and page 15, lines 4-7. The processor further temporarily releases operational control of the electrical load so that the electrical load continues to operate in an open control mode while application code is loaded to the memory location (such as step 3 in FIG. 8 and step 258, FIG. 9) – see specification at page 10, lines 16-23; page 11, lines 20-25; page 15, lines 9-11; and page 16, lines 16-25. The processor further resumes operational control of the electrical load using the application code (such as step 4 in FIG. 8 and step 260, FIG. 9) – see specification at page 11, lines 26-31; page 13, lines 24-28; and page 15, lines 11-14.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. The final rejection of claims 1-2, 6-7 and 19-20 under 35 U.S.C. §102(e) as being anticipated by U.S. Published Patent Application No. US2004/0019776A1 to Sato et al. ("Sato '776") is presented as a first grounds of rejection to be reviewed on appeal.

2. The final rejection of claims 3-5 and 8-18 under 35 U.S.C. §103(a) as being obvious over Sato '776 in view of U.S. Patent No. 6,405,311 to Broyles et al. ("Broyles '311") is presented as a second grounds of rejection to be reviewed on appeal.

The claims do not stand or fall together, but rather will be argued separately in accordance with the following groupings:

1. First Group of Claims: Claims 1-2, 6-7 and 19-20
2. Second Group of Claims: Claims 3-5
3. Third Group of Claims: Claims 8-13
4. Fourth Group of Claims: Claims 14-18

VII. ARGUMENT

A. PATENTABILITY OF FIRST GROUP CLAIMS 1-2, 6-7 AND 19-20

Independent claim 1 generally features steps of *"controlling an electrical load with a first code executed by a processor; releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code; and reinstating processor control of the electrical load using the second code."*

The anticipation rejection of claim 1 is improper including on the basis that Sato '776 fails to carry out the "releasing" step as claimed, as well as on the basis that the Examiner has mischaracterized several aspects of Sato '776.

SATO '776 FAILS TO DISCLOSE "RELEASING PROCESSOR CONTROL" AS CLAIMED BY CLAIM 1

As the Board will appreciate, a *prima facie* case of anticipation under §102 requires each limitation of the claim to be identically arranged in a single prior art reference, either explicitly or via inherency. *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990); MPEP 2131.

Inherency is met only if the skilled artisan would *necessarily* find the missing limitation to nevertheless be present in the cited reference. *Continental Can v. Monsanto*, 20 USPQ2d 1746 (Fed. Cir. 1991); MPEP 2112.

Further, no *prima facie* case of anticipation can be established when the rejection is based on a substantive mischaracterization of the actual disclosure of the prior art reference. See *Bond, Supra*; *In re Cortright*, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999)(*terms used in the cited reference must be interpreted in accordance with the understanding of the skilled artisan*); MPEP 2111.

In the present case, Sato '776 at least fails to disclose the step of "*releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code,*" as claimed by claim 1. See Applicant's Response filed November 27, 2006, pp. 7-9. Sato '776 discloses the application of continuous processor control of the electrical load throughout the initialization process, so that no "releasing" of processor control takes place as claimed.

Sato '776 generally discloses a disk drive with a disk controller 110, 410 comprising a disk controlling section 411 and a processor 412. See FIGS. 3 and 6; paras [0006] and [0077].

The processor 412 generally operates to initialize the disk drive by executing a boot program from ROM 413. Paras [0008] and [0079]. The boot program controls the loading of a main program from a disk 101 to RAM 414 via a program loading section 417. See FIG. 3 and paras [0008], [0087]-[0088]. Once the main program has been loaded the processor 412 immediately switches operational control from the boot program to the main program. FIG. 5, step 307; paras [0009], [0082] and [0092]. This transfer of operational control is

disclosed as being carried out by the execution of a "*branch instruction or the like*" in the boot program. See para [0082], lines 10-15.

Those with skill in the art would recognize that the execution of the boot program involves the sequential execution of each instruction in the boot program in turn. When the boot program step involving the "*branch instruction or the like*" is reached, the processor immediately executes the first instruction in the main program. The skilled artisan would thus view this process as being under constant processor control, and no "*releasing*" of processor control takes place "*while the first code is displaced with a second code.*"

SATO '776 FAILS TO DISCLOSE OPERATION OF THE RECITED ELECTRICAL LOAD IN AN "OPEN CONTROL MODE" AS CLAIMED BY CLAIM 1

Claim 1 recites that the "*releasing processor control*" step occurs such that "*the electrical load operates in an open control mode while the first code is displaced with a second code.*" This operation is not disclosed by Sato '776.

As discussed more fully in the Applicant's Response filed November 27, 2006, Sato '776 discloses that the electrical load (spindle motor 404) is continuously operated under processor control in a closed control mode during the entire device initialization process. See Response, pp. 7-8; Sato '776, para [0006] and FIG. 6.

The disk controlling section 411 of FIGS. 3 and 6 operates to exchange control data between the processor 412 and the spindle motor 404. (*"A disk controlling section 411 intermediates exchange of control data on the operation of a hardware section between a processor 412 and the hardware section..."* Sato '776, para. [0006], lines 1-7). The phrase "exchange of control data" indicates to the skilled artisan that the disk controlling section 411

is a conduit to enact commands by the processor 412 (e.g., accelerate the motor 404) and to report back to the processor ongoing status data (e.g., present speed of the motor 404) during processor control of the hardware section.

It is in this context that Sato '776 describes the operation of the processor 412 and the disk controlling section 411 during the boot process of FIG. 5. At step 301 in FIG. 5, the processor 412 commands the disk controlling section 411 to accelerate the spindle motor 404 to a common rotational speed. Para [0085].

At decision step 302 in FIG. 5, the processor 412 performs closed loop monitoring of the progress of the motor acceleration, and continues to wait until the desired motor speed has been achieved. Para [0086]. Sato '776 describes this process as follows:

> *Thereafter, the common boot section 211* [of the processor 412] repeats Step 302 and waits for *stabilization of the rotation speed of the disk 101. Then, when notified, via the disk controlling section 411, of the fact that the spindle motor 404 now steadily drives at the above-described common rotation speed, the common boot section 211 determines as an affirmative judgment of Step 302 that the spindle motor 404 has completed the acceleration, and proceeds to Step 303.* Para [0086], lines 1-8 (emphasis added)

The skilled artisan would view this operation to be under constant processor control. The processor 412 commands the desired target speed; receives notification by the disk controlling section 411 that the motor has reached the desired speed; upon such notification, makes an affirmative judgment that the desired speed has been reached; and then proceeds with the next step in the routine after making this affirmative judgment. It is further noted that the processor 412 does not carry out any other operations during the waiting phase of step 302.

In view of the description of the data exchange operation between the disk controlling section 411 and processor 412 in para [0006], the skilled artisan would further understand that such closed loop monitoring and reporting of the spindle motor speed continues throughout the rest of the routine of FIG. 5.

In a similar fashion, step 303 of FIG. 5 of Sato '776 discloses a command by the processor 412 to move the associated transducer to the disk system area that stores the main program. Para [0086], lines 9-11. The processor 412 again monitors this operation at decision step 304 and waits for explicit notification that the transducer is over the desired area, and makes an affirmative judgment to this effect. Para [0087], lines 1-6. At this point, the processor commands the transfer of the main program to RAM 414 at step 305. Para [0087], lines 7-9. Again, the skilled artisan would readily view this as under constant processor control, with no "releasing" of processor control taking place either during or after this process.

In contravention of this clear disclosure of Sato '776, however, the Examiner had the temerity to state as follows:

> *Applicant argues in substance that Sato, at paragraph [0006] lines 1-7 intermediates exchange of control data on the operation of a hardware section between a process and the hardware section and thus is not in an open control mode. The examiner respectfully disagrees. The portion of Sato to which the Applicant refers is in the background of Sato and is thus prior art. The prior art does not have any handover of code from a first code to a second code and thus this portion of Sato cannot be used with his preferred embodiments.* Advisory Action mailed December 19, 2006, p. 2, lines 3-6 (emphasis added)

This statement is respectfully traversed for a number of reasons. First of all, while it may be true that FIG. 6 and paragraph [0006] et seq. are in the background section of Sato '776, the "prior art" hardware section described therein does in fact carry out a handover of

code from a first code to a second code. See Sato '776 paras [0008] and [0009] where Sato '776 explicitly describes operation of a "boot program" followed by transition to a "main program." Those with skill would readily discern that the "boot program" is a first code and the "main program" is a second code, and a "handover" indeed takes place from the former to the latter.

FIG. 6 of Sato '776 shows a "program loading section 417" which operates as described by Sato '776 to *load* the second code (i.e., the main program). It is difficult to see how the Examiner could reasonably assert that FIG. 6 does not involve any handover from a first code to a second code, when FIG. 6 has a processor module explicitly labeled as "program loading section 417" that facilitates this very operation. Indeed, the Applicant wonders what a "program loading section" is for, if not to load a program.

More importantly, though, Sato '776 expressly states that with regard to the drawings, "*like parts* are designated by *identical reference numbers*." Para. [0037]. One with skill would understand this to mean that if the same component reference numeral appears in multiple figures, the components are intended to be the same in each figure. Thus for example, if a component labeled and numerically denoted in prior art FIG. 6 is also presented in FIG. 3, then it would be expected that the component would be a "like part" and would operate the same way in both figures.

The Applicant notes that the "disk controlling section 411" appears in both FIGS. 3 and 6. Thus, contrary to the Examiner's contention, the discussion of the disk controlling section 411 provided by Sato '776 with respect to FIG. 6 is wholly applicable to the operation of this same component in FIG. 3. It is noted that this also applies to the "mask

ROM 413," "RAM 414," "interface controller 415," "program loading section 417," and "normal operation section 418," all of which are present in both FIGS. 3 and 6 of Sato '776.

Accordingly, the Examiner has substantively contradicted the clear disclosure of Sato '776 and has based the rejection of independent claim 1 on this mischaracterization. No *prima facie* case of anticipation therefore has been made, and the rejection should be withdrawn on this basis as well. *In re Cortright, Supra.*

THE EXAMINER IMPROPERLY SPECULATES THAT COMPLETION OF A COMMANDED STATE NECESSARILY RESULTS IN RELEASE OF PROCESSOR CONTROL AS CLAIMED

The Examiner has further taken the position that, to the extent that the operation of decision steps 302 and 304 in FIG. 5 of Sato '776 might be viewed as disclosing periods of processor control, the conclusion of these respective steps necessarily result in a "releasing" of processor control as claimed. Specifically, the Examiner stated as follows:

> *Applicant argues in substance that there is nothing in Sato that teaches or suggests that the disk controlling section [section 411] stops sending speed control data to the processor once step [302 is completed] and rather that the skilled artisan would view this data as being continuously provided by the section 411 to the processor for use in the processor's top level control for the entire storage system. The examiner disagrees. Applicant is directed to paragraph [0086], which discloses that the spindle motor now steadily drives at the common rotation speed. Thus, one of ordinary skill in the art would understand that no further control is required and further that step 302 has been completed [is] no longer required.* Advisory Action, p. 2, lines 12-17.

As noted above, this position by the Examiner is directly contrary to the express disclosure of Sato '776 at para [0006] *et seq*. As discussed previously by the Applicant in the Response to Final Office Action filed November 27, 2006 at pp. 8-9, the recited "*open*

control mode" is not achieved merely by the load achieving a processor commanded state.

Rather, "*open control mode*" requires an affirmative prior "*releasing*" of processor control before the "*open control mode*" is enacted. Such "*open control mode*" also requires that the load operate without "*further processor regulation or intervention*" during such mode. Specification of the present application, page 16, lines 16-21; Applicant's 11/26/06 Response, p. 8.

The inquiry is thus not whether Sato '776 discloses to command a state and achieves the same; the inquiry is whether Sato '776 discloses that proeessor control is released such that "*the electrical load operates in an open control mode while the first code is displaced with a second code,*" as claimed. Sato '776 is clearly silent on this point, as the Examiner tacitly admits.

For example, the Examiner cannot determine whether the processor 412 would respond to a notification of subsequent failure of the motor 404 – this is something that, according to the Examiner, "*cannot be determined from Sato.*" See Advisory Action, p. 2, lines 19-21; Applicant's 11/26/06 Response, p. 10.

By this the Examiner admits that he cannot tell whether the spindle motor 404 is actually operating in an "*open control mode*," as claimed. The recited "*open control mode*" is therefore not necessarily present in Sato '776, which would be required to establish anticipation via inherency. *Continental Can, Supra.*

The Examiner has accordingly failed to show either explicitly or inherently that Sato '776 discloses a step of "*releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code.*" The burden is upon the Examiner to establish this operation is disclosed by the reference, not upon the

Applicant to show that it is absent. Since Sato '776 expressly identifies a continuous data exchange between the disk controlling section 411 and processor 412, the Examiner's speculation that no processor regulation or intervention would occur has no weight. Reconsideration and withdrawal of the rejection are respectfully requested on this basis as well.

B. PATENTABILITY OF SECOND GROUP CLAIMS 3-5

Dependent claims 3-5 depend from claim 1, and were rejected under §103(a) as obvious over Sato '776 in view of Broyles '311. These claims are argued separately because of the different basis for rejection. The dependent claims 3-5 are submitted as being patentable as depending from a patentable base claim, and reconsideration and withdrawal of the §103(a) rejection of these claims are requested on this basis.

C. PATENTABILITY OF THIRD GROUP CLAIMS 8-13

Independent claim 8 generally features "*using a processor to execute startup code loaded into a memory location to initiate operational control of an electrical load; continuing to operate the electrical load while processor operational control of the electrical load is temporarily suspended to load application code to the memory location; and resuming operational control of the electrical load using the application code.*"

Claim 8 stands finally rejected as being obvious over Sato '776 in view of Broyles '311. This is respectfully traversed on the following bases.

THERE IS NOTHING IN THE CITED REFERENCES THAT WOULD SUGGEST THE DESIRABILITY, AND THUS THE OBVIOUSNESS, OF MODIFYING THE REFERENCES TO ARRIVE AT THE SUBJECT MATTER OF CLAIM 8

Obviousness is determined by the USPTO in view of the factual inquires and secondary considerations set forth by *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966). The claimed invention must be considered as a whole, the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination, the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and a reasonable expectation of success must be shown. See MPEP 2141.

With regard to the claimed subject matter, there is nothing in Sato '776 or Broyles '311, alone or in combination, that would suggest the desirability of modifying and/or combining these references to arrive at the claimed subject matter.

When considering the claimed subject matter of claim 8 as a whole (per *Graham*), the skilled artisan would note that claim 8 generally includes the express step of "*continuing to operate the electrical load while processor operational control of the electrical load is temporarily suspended to load application code to the memory location.*"

As discussed previously by the Applicant in the 11/26/06 Response at pp. 9-11, the claim term "operational control" is defined in the specification of the present application as a mode "*whereby the processor engages in continual active regulation, intervention or verification to maintain the continued operation of the load, or simply a mode where the processor controls the load.*" Specification, page 16, lines 22-25. To "temporarily suspend" such operational control would thus require a cessation of such regulation, intervention,

verification or control. This is supported, for example, in the specification at page 10, lines 16-23.

Next, when considering Sato '776 as a whole (per *Graham),* this reference maintains continuous processor operational control of the loads (e.g., spindle motor 404) during the loading of the main program, and uses a "*branch instruction or the like*" to transition from the last boot program instruction to the first main program instruction. Paras [0008], [0087]-[0088]. It is apparent that throughout such operation, the disk monitoring section 411 provides continual exchange of control data with the processor 412, which would be viewed by the skilled artisan as providing continual "operational control."

Moreover, a careful review of Sato '776 as a whole shows that the novelty presented by the embodiment of FIG. 3 of Sato '776 involves steps that take place *after* control has already been transferred to the main program; that is, the main program merely incorporates additional steps of determining whether a further speed increase is warranted, and if so, executes the same. See steps 308-311 in FIG. 5 and paras [0089]-[0092]. As with the prior art system of FIG. 6 of Sato '776, the new embodiment of FIG. 3 of Sato '776 does not involve any type of "temporary suspension" of operational control with regard to the electrical load, as claimed, nor is there anything to suggest the desirability of carrying out such temporary suspension, as claimed.

Similarly, considering Broyles '311 as a whole (per *Graham*) shows that this reference merely discloses a nonvolatile memory (flash ROM 78) with a revision indicator that maintains a revision level for hardware present in a computer system S. See FIGS. 1-2, col. 3, lines 21-35; col. 5, lines 59-65. The revision indicator may be referenced during a

powerup sequence in which a boot program is executed, followed by a system level operating system (OS). See FIG. 5.

Accordingly, there is nothing in Sato '766, in Broyles '311, or in the art in general, that would suggest the desirability of modifying and/or combining the references to arrive at the method as claimed by claim 8, as required to establish a *prima facie* case of obviousness.

THERE IS NO EVIDENCE OF RECORD THAT THE SKILLED ARTISAN WOULD HAVE A "REASONABLE EXPECTATION OF SUCCESS" IN MODIFYING AND/OR COMBINING THE CITED REFERENCES TO ARRIVE AT THE SUBJECT MATTER OF CLAIM 8

A separate showing is required to establish evidence that the skilled artisan would have a "reasonable expectation of success" in making such combination. *Graham, Supra;* MPEP 2141. No such showing has been established by the Examiner, nor can be established, with regard to either Sato '776 or Broyles '311, for the reasons set forth above.

Further, neither reference even recognizes the problem solved by the claimed subject matter, much less supports a view that a skilled artisan would have a reasonable expectation of success in modifying the references to arrive at the claimed combination. Accordingly, per *Graham*, the inventive subject matter of claim 8 stands patentable over these references on this basis as well.

C. PATENTABILITY OF FOURTH GROUP CLAIMS 14-18

Independent claim 14 generally features "*a programmable processor*" which "*executes startup code loaded into the memory location to initiate operational control of the load, temporarily releases operational control of the electrical load so that the electrical load continues to operate in an open control mode while application code is loaded to the*

memory location, and resumes operational control of the electrical load using the application code."

As with claims 8-13, the Applicant respectfully submits that no *prima facie* case of obviousness of independent claim 14 has been established by the Examiner in view of Sato '776 and Broyles '311.

THERE IS NOTHING IN THE CITED REFERENCES THAT WOULD SUGGEST THE DESIRABILITY, AND THUS THE OBVIOUSNESS, OF MODIFYING THE REFERENCES TO ARRIVE AT THE SUBJECT MATTER OF CLAIM 14

When considering the claimed subject matter of claim 14 as a whole (per *Graham*), the skilled artisan would note that claim 14 generally includes a processor which "*temporarily releases operational control of the electrical load so that the electrical load continues to operate in an open control mode while application code is loaded to the memory location.*"

The skilled artisan would find this language of claim 14 to include a temporary release of "*operational control*," and an operation of the load in "*open control mode*," while the "*application code is loaded to the memory location.*" These respective claim terms would be understood as discussed above.

When considering Sato '776 as a whole (per *Graham*), it can be readily seen that the transfer of the main program from disk to RAM 414 is carried out under the direction of the program loading section 417 of processor 412. See FIG. 3, and para [0088]. As noted above, there is nothing that could be reasonably construed from Sato '776 to indicate that the processor 412 maintains constant control with the disk monitoring section 411 sufficient to

transfer the main program from disk, while *at the same time* releasing operational control of the spindle motor 404 during this transfer.

Rather, the express teachings at para [0006] *et seq.* of continual data exchanges between the disk monitoring section 411 and the processor 412 would indicate to the skilled artisan that operational control of the spindle motor 404 is also maintained by the processor 412 during this data transfer sequence. There is certainly nothing of record, other than the Examiner's unsupported speculations, to indicate otherwise.

Thus, when considering Sato '776 as a whole, continual active operational control is maintained during the loading of the main program, which is directly contrary to the language of claim 14. It is believed this would generally tend to weigh against a finding of "desirability to modify/combine" the Sato '776 reference.

Similarly, considering Broyles '311 as a whole (per *Graham*) shows that this reference provides nothing to indicate that operational control of a load is temporarily released during transfer of OS code, or any other code for that matter, to the RAM. FIG. 5; col. 8, lines 46-51.

Accordingly, there is nothing in Sato '766, in Broyles '311, or in the art in general, that would suggest the desirability of modifying and/or combining the references to arrive at the system as claimed by claim 14, as required to establish a *prima facie* case of obviousness.

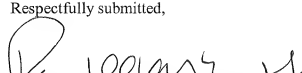
THERE IS NO EVIDENCE OF RECORD THAT THE SKILLED ARTISAN WOULD HAVE A "REASONABLE EXPECTATION OF SUCCESS" IN MODIFYING AND/OR COMBINING THE CITED REFERENCES TO ARRIVE AT THE SUBJECT MATTER OF CLAIM 14

As with claim 8, there is similarly nothing of record to support a conclusion that the skilled artisan would have a "reasonable expectation of success" in combining/modifying the references to arrive at the subject matter of claim 14. *Graham, Supra;* MPEP 2141. Accordingly, per *Graham*, the inventive subject matter of claim 14 stands patentable over these references on this basis as well.

Conclusion

For the foregoing reasons, the Applicant respectfully submits that claims 1-20 define subject matter that is patentable over the art of record, and respectfully requests that the Board reverse the final rejection of claims 1-20.

Respectfully submitted,

By: 

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VIII. CLAIMS APPENDIX

1. (Original) A method, comprising:

controlling an electrical load with a first code executed by a processor;

releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code; and

reinstating processor control of the electrical load using the second code.

2. (Original) The method of claim 1, wherein the first code of the controlling step is supplied from a boot read only memory (ROM).

3. (Original) The method of claim 1, wherein the controlling step comprises loading the first code into a first memory location accessed by the processor.

4. (Original) The method of claim 3, wherein the controlling step further comprises loading the second code into a second memory location accessible by the processor.

5. (Original) The method of claim 4, wherein the releasing step comprises moving the second code from the second memory location into the first memory location, thereby displacing the first code from the first memory location.

6. (Original) The method of claim 1, wherein the electrical load is a motor.

7. (Original) The method of claim 6, wherein the motor supports a data storage medium, and wherein the controlling step comprises using the motor to rotate the data storage medium at an operational velocity and retrieving the second code from the rotating data storage medium.

8. (Previously presented) A method, comprising:

using a processor to execute startup code loaded into a memory location to initiate operational control of an electrical load;

continuing to operate the electrical load while processor operational control of the electrical load is temporarily suspended to load application code to the memory location; and

resuming operational control of the electrical load using the application code.

9. (Original) The method of claim 8, wherein the startup code of the using step is supplied from a boot read only memory (ROM).

10. (Original) The method of claim 8, wherein the memory location of the using step is characterized as a first memory location, and wherein the using step further comprises loading the application code into a second memory location accessible by the processor.

11. (Original) The method of claim 10, wherein the continuing step comprises moving the application code from the second memory location into the first memory location, thereby displacing the startup code from the first memory location.

12. (Original) The method of claim 8, wherein the electrical load comprises a motor supporting a data storage medium, and wherein the using step comprises energizing the motor to rotate the data storage medium at an operational velocity and retrieving the application code from the rotating data storage medium.

13. (Original) The method of claim 12, wherein the using step further comprises using the startup code to energize an actuator motor to bring a data transducing head into alignment with a track defined on the data storage medium, and utilizing the head to transduce the application data from said track.

14. (Previously presented) An apparatus, comprising:

an electrical load;

a memory location; and

a programmable processor coupled to the memory location and adapted to control the electrical load, wherein during an initialization process the processor executes startup code loaded into the memory location to initiate operational control of the load, temporarily releases operational control of the electrical load so that the electrical load continues to operate in an open control mode while application code is loaded to the memory location, and resumes operational control of the electrical load using the application code.

15. (Original) The apparatus of claim 14, further comprising a boot read only memory (ROM) which stores the startup code, wherein the startup code is loaded from the boot ROM to the memory location for execution by the processor.

16. (Original) The apparatus of claim 14, wherein the memory location of the using step is characterized as a first memory location, and wherein the apparatus further comprises a second memory location accessible by the processor and into which the processor loads the application code.

17. (Original) The apparatus of claim 14, wherein the electrical load comprises a motor supporting a data storage medium, and wherein the execution of the startup code by the processor results in the energizing of the motor to rotate the data storage medium at an operational velocity.

18. (Original) The apparatus of claim 17, further comprising an actuator motor coupled to a data transducing head, and wherein the execution of the startup code by the processor further results in the energizing of the actuator motor to bring the head into alignment with a track defined on the data storage medium, the head transducing the application data from said track.

19. (Previously presented) The method of claim 1 wherein the processor operationally controls the electrical load.

20. (Previously presented) The method of claim 1, wherein at least one control signal is applied to the electrical load during the open control mode of the releasing step.

IX. EVIDENCE APPENDIX

No additional evidence is included.

X. RELATED PROCEEDINGS APPENDIX

There exist no relevant related proceedings concerning this Appeal before the Board.